

✓

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : ASAI Motoo et al.
Application No. : 09/319,258
I.A. Filed : December 18, 1997
For : PRINTED WIRING BOARD AND METHOD FOR
MANUFACTURING THE SAME

VERIFICATION OF TRANSLATION


Honorable Commissioner of Patents and Trademarks
Washington D.C. 20231

Sirs:

Yoshikazu KASAI, of #906, 7-19, Tsurugamine 2-Chome, Asahi-Ku,
Yokohama-Shi, Kanagawa, 241-0022 Japan
declares:

- (1) that I know well both the Japanese and English languages;
- (2) that I have translated the Japanese Patent Application No. 9-29587 from Japanese to English;
- (3) that the attached English translation is a true and correct translation of the Japanese Patent Application No. 9-29587 to the best of my knowledge and belief; and
- (4) that all statements made of my own knowledge are true and that all statements made of information and belief are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and that such false statement may jeopardize the validity of the application or any patent issuing thereon.

October 21, 2002


Translator: Yoshikazu KASAI

English Translation
Japanese Patent Application No. 9-29587

[Identification of the Document] Patent Application

[Reference Number] H08HOAD009

[Date of Submission] January 28, 1997

[Addressee] Director-General of the Patent Office

[International Patent Classification] H05K 3/00

[Title of Invention]

Method of forming a solder bump on a
printed circuit board, a printed circuit board, and a
mask for printing

[Number of Claims] 7

[Inventor(s)]

[Address]

c/o IBIDEN Co., Ltd. 1-1, Kitakata,
Ibigawa-cho, Ibi-gun, Gifu

[Name] YAMADA Kazuhito

[Inventor(s)]

[Address]

c/o IBIDEN Co., Ltd. 1-1, Kitakata,
Ibigawa-cho, Ibi-gun, Gifu

[Name] WAKIHARA Yoshinori

[Applicant(s)]

[Identification Number] 000000158

[Name] IBIDEN Co., Ltd.

[Representative] ENDOH Masaru

[Representative]

[Identification Number] 100095832

[Patent Attorney]

[Name] HOSODA Yoshinori

[List of Attached Items]

[Identification of Item] 1 Copy of Specification

[Identification of Item] 1 Copy of Drawings

[Identification of Item] 1 Copy of Abstract

[General Authorization Number] 9201997

[Identification of the Document]
Specification

[Title of the Invention]

Method of forming a solder bump on a printed circuit board, a printed circuit board, and a mask for printing

[Scope of Claims for Patent]

[Claim 1]

A method of forming a solder bump on a printed circuit board comprising the steps of:
 laminating a mask for printing provided with an alignment mark for positioning relative to an opening portion for solder printing and a printed circuit board on the printed circuit board provided with an alignment mark for positioning relative to the mask for printing;
 adjusting both the alignment marks;
 printing a cream solder on a semiconductor element mounting portion of the printed circuit board; and
 heating and solder-dissolving to form the solder bump on the printed circuit;
 characterized in that
 the adjusting step comprising,
 the alignment mark provided on the mask for printing being a through-hole, and the alignment mark provided on the printed circuit board being formed on a portion in the vicinity of an outer peripheral portion of the printed circuit board where no conductor pattern is formed.

[Claim 2]

A method of forming a solder bump on a printed circuit board according to claim 1. wherein the alignment mark formed on the portion in the vicinity of the outer peripheral portion where no conductor pattern is formed being cut and removed after forming a solder bump.

[Claim 3]

A printed circuit board having an alignment mark comprising a conductor layer used for positioning a mask for printing, characterized in that
 the alignment mark is formed on a portion in the vicinity of an outer peripheral portion of the printed circuit board where no conductor pattern is formed.

[Claim 4]

A printed circuit board according to claim 3, wherein the alignment mark is formed with an opening portion exposed only to the surface of the conductor layer from a solder resist layer formed on the conductor layer.

[Claim 5]

A printed circuit board according to claim 3 or 4, wherein the surface of the conductor is provided with a roughened layer.

[Claim 6]

A printed circuit board according to any one of claims 3-5, wherein a metal layer of nickel-gold is formed on the conductor layer exposed from the opening portion.

[Claim 7]

A printed mask provided with an opening portion for solder printing and an alignment mark for positioning relative to a printed circuit board, characterized in that the alignment mark is formed with a through-hole at a position corresponding to a portion in the vicinity of an outer peripheral portion of the printed circuit board where no conductor pattern is formed.

[Detailed Explanation of the Invention]

[0001]

[Technical Field where the Invention belongs to]

The invention relates to a solder bump formation on a printed circuit board. More specifically, the invention relates to a method of forming a solder bump by printing a cream solder on a semiconductor element mounting area provided on the printed circuit board and reflowing it to form a solder bump, a printed circuit board, and a mask for printing.

[0002]

[Prior Art]

In general, an IC chip mounting portion on the surface of a printed circuit board is formed with a ball group of solders named as solder bump, and an IC chip is mounted on the printed circuit board by placing the IC chip on the solder bump and heating.

[0003]

Hitherto, as a method of forming a solder bump, there is adopted a method wherein an alignment mark is previously formed on a mask for printing such as a metal mask, a plastic mask or the like and a printed

circuit board in order to determine positioning of the mask for printing and the printed circuit board, and then both alignment marks are adjusted to each other to laminate the mask for printing on the printed circuit board at a given position, and thereafter a cream solder is printed thereon.

With the recent refinement of circuit board, it is necessary to shorten the height of a solder bump, so as to make the thickness of a printed mask thin, and as a result, an alignment mark should be a through-hole.

[0004]

Moreover, as an alignment mark for the positioning relative to a mask for printing of a printed circuit board, use is made of an alignment mark 13 for mounting an IC chip provided in a product portion of the printed circuit board. A cream solder is printed on an IC chip mounting alignment mark 130 of the printed circuit board from an alignment mark comprised of a through-hole of the mask for printing, therefore, the alignment mark cannot be recognized, and the IC chip cannot be mounted on the printed circuit board (see Fig. 6).

[0005]

[Problem to be solved by the Invention]

The invention is made in light of the conventional technique, and aims to enable the IC chip to be mounted even if a cream solder is printed on an alignment mark for positioning relative to the printed circuit board.

[0006]

[Means for solving the Problem]

The gist of the invention relates to:

(1) A method of forming a solder bump on a printed circuit board comprising the steps of:

laminating a mask for printing provided with an alignment mark for positioning relative to an opening portion for solder printing and a printed circuit board on the printed circuit board provided with an alignment mark for positioning relative to the mask for printing;

adjusting both the alignment marks;

printing a cream solder on a semiconductor element mounting portion of the printed circuit board; and

heating and solder-dissolving to form the solder bump on the printed circuit;

characterized in that

the adjusting step comprising,

the alignment mark provided on the mask for printing being formed with a through-hole, and

the alignment mark provided on the printed circuit board being formed on a portion in the vicinity of an outer peripheral portion of the printed circuit board where no conductor pattern is formed,

(2) A method of forming a solder bump on a printed circuit board described in (1), wherein the alignment mark formed on the portion in the vicinity of the outer peripheral portion where no conductor pattern is formed being cut and removed after forming a solder bump,

(3) A printed circuit board provided with an alignment mark comprised of a conductor layer used for positioning relative to a mask for printing, characterized in that the alignment mark is formed on a portion in the vicinity of an outer peripheral portion of the printed circuit board where no conductor pattern is formed,

(4) A printed circuit board described in (3), wherein the alignment mark is formed with an opening portion exposed only to the surface of the conductor layer from a solder resist layer formed on the conductor layer,

(5) A printed circuit board described in (3) or (4), wherein the surface of the conductor is provided with a roughened layer,

(6) A printed circuit board described in any one of (3-5), wherein a metal layer of nickel-gold is formed on the conductor layer exposed from the opening portion, and

(7) A printed mask provided with an opening portion for solder printing and an alignment mark for positioning relative to a printed circuit board, characterized in that the alignment mark is formed with a through-hole at a position corresponding to a portion in the vicinity of an outer peripheral portion of the printed circuit board where no conductor pattern is formed.

[0007]

[Mode for carrying out the Invention]

The invention relates to a method of forming a solder bump on a printed circuit board, comprising the steps of laminating a mask for printing provided with an alignment mark for positioning an opening portion for solder printing and a printed circuit board on the printed circuit board provided with an alignment mark for positioning the mask for printing, adjusting both the

alignment marks, printing a cream solder on a semiconductor element mounting portion of the printed circuit board, and heating and solder-dissolving to form a solder bump on the printed circuit, characterized in that the alignment mark provided on the mask for printing is formed with a through-hole, and the alignment mark provided on the printed circuit board is formed on a portion in the vicinity of an outer peripheral portion of the printed circuit board where no conductor pattern is formed.

Moreover, a printed circuit board used in a method of forming a solder bump according to the invention, in the printed circuit board provided with an alignment mark comprised of a conductor layer used for positioning to a mask for printing, is characterized in that the alignment mark is formed on a portion in the vicinity of an outer peripheral portion of the printed circuit board where no conductor pattern is formed.

Furthermore, the mask for printing used in a method of forming a solder bump according to the invention is a mask for printing provided with an opening portion for solder printing and an alignment mark for positioning to the printed circuit board, characterized in that the alignment mark is formed with a through-hole at a position corresponding to a portion in the vicinity of an outer peripheral portion of the printed circuit board where no conductor pattern is formed.

[0008]

Fig. 1 is a rough explanatory view showing one embodiment of a method of forming a solder bump of a printed circuit board according to the invention, but the invention is not limited to such embodiment.

In Fig. 1(b), 1 is a mask for printing, and such mask for printing 1 is formed with an opening portion (through-hole) 3 for solder printing and an alignment mark 4 for positioning to a printed circuit board 5 at a position corresponding to a pad of a metal substrate 2.

[0009]

A mask for printing 1 is not particularly limited and any conventional material can be used. The mask for printing 1 is made of a metal, for example, nickel alloy, nickel-cobalt alloy, stainless steel and the like; or made of resin such as polyimide resin and the like and so forth, but the invention is not limited to such material as illustrated. Preferably, among them, in view of cost, durability, accuracy of an opening portion and the like,

nickel alloy and nickel-cobalt alloy are desirable.

[0010]

A thickness of the mask for printing 1 is not particularly limited, but is generally about 30~150 μm , preferably about 40~80 μm .

[0011]

An opening portion 3 of the mask for printing 1 is, in a metal substrate 2, generally, provided at a position corresponding to a pad 11 for forming a solder bump of a printed circuit board 5.

[0012]

The shape, size and the like of the opening portion of the mask for printing 1 are not particularly limited, but optional. As an example, mention can be made of a circle and the like of about 100~200 μm in diameter.

[0013]

The opening portion of the mask for printing 1 can, for example, be formed by an etching process, an additive process, a laser working process and the like. In these processes, the additive method is particularly desirable in consideration of looseness of the cream solder caused by rough sectional shape of the opening portion 3.

[0014]

An alignment mark 4 is for positioning to a printed circuit board 5, in the metal substrate 2, generally, and is provided at a position corresponding to an alignment mark 12 provided on the printed circuit board 5. A number of the alignment mark 4 is optional, and its position is appropriately selected according to the alignment mark 12 of the printed circuit board 5. The invention is characterized by forming the alignment mark on the position corresponding to a portion in the vicinity of the outer peripheral of the printed circuit board 5 where no conductor pattern is formed.

[0015]

As the alignment mark 4, it should be a through-hole. It is desirable to make a mask for printing thin for decreasing a solder amount, but if the mark is made thin, it is difficult to fill resin therein by half etching, and it is advantageous to form an alignment mark by providing a through-hole. In the invention, since the alignment mark 12 of the printed circuit board 5 is formed on the portion where no

conductor pattern is formed in the vicinity of an outer peripheral portion of the printed circuit board, because of IC chip mounting, an alignment mark 13 can mount the IC chip without exerting any influence.

[0016]

The through-hole can, for example, be formed together with an opening portion 3 when the opening portion 3 is formed on the metal substrate 2. A size of the through-hole is not particularly limited, but for example, a diameter of 0.5-1.5 mm, particularly a diameter of 0.8-1.0 mm is preferable.

[0017]

In Fig. 1(a), the printed circuit board 5 is comprised of an insulating base 6, a first layer conductor circuit 8 and an interlaminar insulating material (adhesive layer for electroless plating) 9 formed thereon, a plating resist 10 formed on the interlaminar insulating material 9, a pad 11 (conductor pattern) for a solder bump formation composing a part of a second layer conductor circuit, an alignment mark 12 for positioning to the mask for printing 1 formed on a non forming portion of the plating resist 10, and an alignment mark 13 for an IC chip mounting, and further alignment marks 12 and 13 formed on the plating resist 10 and a solder resist layer 14 for protecting a portion other than the pad 11 for the solder bump formation.

[0018]

In Fig. 1(a), the conductor circuit of the printed circuit board 5 is a multilayered one formed by so-called build-up method, but such conductor circuit may be single-layered one.

[0019]

As the insulating base or substrate 6, for example, mention may be made of resin substrate, ceramic substrate, glass substrate, thin film substrate and the like, but the invention is not limited to such a material. A thickness of the insulating base 6 is not particularly limited to, but generally, about 0.1-2 mm is preferable.

[0020]

The alignment mark 12 used for positioning relative to the mask for printing is formed on a portion where no conductor pattern is formed in the vicinity of an outer peripheral portion of the printed circuit board. Concretely, it is formed, for example, on the outside of a product portion A shown in Fig. 1 and Fig. 2. In the

specification, an outer peripheral portion means the outside portion of such a product portion A. Further, the alignment mark 13 for the IC chip mounting is formed at every product portion in the printed circuit boards in order to mount an IC chip at every product portion.

Therefore, in a method of the solder bump formation according to the invention, even if a cream solder 15 is printed on the alignment mark 12, the cream solder is not printed on the alignment mark 13, and it is possible to mount an IC chip.

[0021]

The shape, size and depth of the alignment mark 12 are not particularly limited, but for instance, a circle of 0.5~1.5 mm in diameter is desirable.

Further, the alignment mark 12 is preferably formed in the opening portion exposed only to the surface of the conductor layer 120 from the solder resist layer 14 formed on the conductor layer 120.

[0022]

The reason is explained with reference to Figs. 3 and 4. In Fig. 3(a), the alignment mark 12 is formed in the opening portion exposed only to the surface of a conductor layer 120 from the solder resist layer 14 formed on the conductor layer 120. That is, as in Fig. 3(d), the peripheral edge of the conductor layer 120 overlaps with the solder resist layer 14, the plating resist 10 and the interlaminar insulating layer 9 around the conductor layer 120 are not exposed from the opening portion of the solder resist layer, and the conductor layer 120 is only exposed.

[0023]

In case of the alignment mark 12, the positioning to the mask for printing is carried out by mainly recognizing the center of the mark as the center of the opening portion. The opening of the solder resist layer is formed by providing a photosensitive resin layer, placing a photo-mask and subjecting to light exposure and developing treatments, but in case of placing the photo-mask, the position of the opening is sometimes shifted.

[0024]

If the position of the opening portion of the solder resist layer 14 is shifted as shown in Fig. 3(b), the center of the opening portion becomes the center of the alignment mark, so that the position of the alignment mark is shifted in compliance with the shifting

amount of the position of the opening portion of the solder resist layer 14, and as a result, the position of the mask for printing is shifted in compliance with the opening position of the solder resist layer 14. Therefore, notwithstanding the shifting of the opening position of the solder resist layer 14, the mask for printing is always coincident with the opening portion of the solder resist layer 14. Hence, a printing amount of the cream solder is not decreased by the solder resist layer 14, and the height of a solder bump can be ensured even if the solder bump is formed by heating and dissolution as shown in Fig. 3(c).

[0025]

However, as shown in Figs. 4(a) and 4(d), when the conductor layer 120 is completely exposed from the solder resist layer, the conductor layer 120 itself becomes the alignment mark 12. The center of the alignment mark 12 is the center of the conductor layer 120.

If the position of the opening portion of the solder resist layer 14 is shifted as shown in Fig. 4(b), the center of the conductor layer 120 becomes the center of the alignment mark, so that even if the position of the opening portion of the solder resist layer 14 is shifted, the position of the alignment mark 12 is not shifted.

Therefore, the mask for printing is placed on the basis of the alignment mark 12, and even if the opening of the solder resist layer 14 and the opening of the mask for printing are shifted and the cream solder 15 is printed as shown in Fig. 4(c), the printing amount is decreased by the solder resist layer 14, and a solder bump is lowered when the solder bump is formed by heating and dissolution.

[0026]

Therefore, the alignment mark 12 shown in Fig. 3 is relatively advantageous.

In the invention, the alignment mark 12 is desirably formed with a roughened layer 7 on the surface of the conductor layer 120. Because the adhesion property to the solder resist layer 14 is excellent. Particularly in case of the alignment mark 12 shown in Fig. 3, the shape of alignment mark 12 is determined by the opening portion of the solder resist layer 14, so that the peeling of the solder resist layer 14 is of advantage because the function of the alignment mark is lost.

[0027]

It is advantageous that the roughened layer 7

is a needle-shaped alloy plated layer of copper-nickel-phosphorus. The roughened layer 7 is formed by an electroless plating. The composition of a plating aqueous solution is desirably to have a copper ion concentration of $2.2 \times 10^{-2} \sim 4.1 \times 10^{-2}$ mol/l, a nickel ion concentration of $2.2 \times 10^{-3} \sim 4.1 \times 10^{-3}$ mol/l and a hypophosphorus acid ion concentration of 0.20~0.25 mol/l.

The film deposited within the above range is needle in the crystal structure and is excellent in the anchor effect. An electroless plating bath may be added with a complexing agent and additives in addition of the above compounds.

[0028]

The composition of the alloy layer deposited from the electroless plating aqueous solution is desirably to be 90~96 wt% of copper, 1~5 wt% of nickel and 0.5~2 wt% of phosphorus. Because the needle-shaped structure is obtained in such a composition ratio.

[0029]

Moreover, the alignment mark 12 can be formed by a semi-additive process as shown in Fig. 5. The semi-additive process is to form an independent conductor circuit by forming an electroless plated film on the surface of an adhesive layer for roughened electroless plating, providing a plating resist therein, subjecting to electrolytic plating, thereafter removing the plating resist and etching the electroless plated film under the plating resist.

[0030]

Therefore, the alignment mark 12 is comprised of an electroless plated film 19 and an electrolytic plated film 18. Further, since the side face of the alignment mark 12 is exposed, a roughened layer 7 can be formed on the side face. When the roughened layer 7 is formed on the side face, generation of cracks in the perpendicular direction in the solder resist layer 14, starting from the boundary of the solder resist layer 14 and the alignment mark 12, can be prevented in the heat cycle.

[0031]

It is desirable to further form a metal layer 16 of nickel-gold on the conductor layer 120 exposed from the opening portion in the alignment mark 12 (it is preferable to form the roughened layer 17 on the surface of the conductor layer as described above). It

is advantageous to coat a gold layer on the surface of the alignment mark 12 because of high reflectance. The formation of the metal layer 16 of nickel-gold can be carried out by electroless plating. It is preferable to have a nickel plating having a thickness of 5 μm , and a flush gold plating having a thickness of 0.1 μm or a gold plating layer having a thickness of 0.5 μm .

[0032]

The first layer conductor circuit 8 may be, generally, two-dimensional or lattice-like shape because it functions as a source layer, a ground layer or the like.

[0033]

As the interlaminar insulating material 9, for example, use is made of an adhesive for electroless plating. As the adhesive for electroless plating, for example, mention can be made of each kind of resins or the like having the insulating property. As a typical example of the resin, for example, mention may be made of epoxy resin, polyimide resin or the like. These resins are cured with a curing agent. Therefore, in case of curing these resins, a curing agent is used. As the curing agent, for example, mention may be made of an imidazole curing agent, an acid anhydride curing agent and the like.

[0034]

Moreover, in the invention, it is desirable to disperse heat-resistant resin particles soluble in acid or oxidizing agent in the interlaminar insulating material 9. In case of dispersing the heat-resistant resin particles within the interlaminar insulating material 9, the surface of the interlaminar insulating material 9 can be roughened, and the adhesion strength of the plating resist 10 to the pad 11 for forming a solder bump can be increased.

[0035]

As the heat-resistant resin particles, for example, mention may be made of not only resin particles comprised of epoxy resin cured with an amine curing agent but also amino resin represented by melamine resin, urea resin, guanamine resin and the like.

[0036]

The heat-resistant resin particles can preferably be used, for example, by selecting from ① heat-resistant resin particles having an average

particle size of not more than 10 μm , ② aggregated particles formed by aggregating heat-resistant primary resin particles having an average particle size of not more than 2 μm , ③ a mixture of heat-resistant resin particles having an average particle size of not more than 10 μm and heat-resistant resin particles having an average particle size of not more than 2 μm , ④ false particles formed by adhering at least one of heat-resistant resin particles having an average particle size of not more than 2 μm and inorganic particles such as silica, alumina, calcium carbonate and the like to the surface of heat-resistant resin particles having an average particle size of 2~10 μm . These resin particles form complicated effect to the plating resist 10 and the pad 11 for forming a solder bump, and can suitably be used in the invention.

[0037]

Moreover, it is desirable to use photosensitive resin for the interlaminar insulating material 9. In case of using the photosensitive resin, a hole and the like for forming a viahole can easily be formed by applying light exposure and developing treatments to the photosensitive resin. As a typical example of the photosensitive resin, for example, mention may be made of epoxyacrylate resin and the like.

[0038]

A thickness of the interlaminar insulating material 9 is not particularly limited, but preferably about 5~100 μm . Moreover, a roughening treatment is applied to the surface of the interlaminar insulating material 9 with the use of, for example, acid, oxidizing agent and the like, by a conventional method.

[0039]

The plating resist 10 is not particularly limited, if it is a generally used one. As the plating resist 10, for example, mention may be made of a composition comprised of epoxyacrylate resin and an imidazole curing agent obtained by reacting epoxy resin and acrylic acid, methacrylic acid and the like; a composition comprised of epoxy acrylate resin, polyether sulfone and an imidazole curing agent and the like. A thickness of the plating resist 10 is not particularly limited, but preferably about 5~40 μm .

[0040]

The pad 11 for forming a solder bump is a part of a second layer conductor circuit and, for example,

formed by electroless plating method and the like. The pad 11 for forming a solder bump is circular, oval, oblong and the like, and formed to make the width larger than that of wiring. A thickness of the pad 11 for forming a solder bump is not particularly limited, but generally desirably about 5~40 μm .

[0041]

As the solder resist layer 14, for example, commercially available ones can be used as they are. For example, it is desirable to use acrylate of epoxy resin and the like, and it is preferable to use coloring matter and pigment such as phthalocyanine green and the like in mixture. A thickness of the solder resist layer 14 is not particularly limited, but for example, desirably about 5~40 μm .

[0042]

The mask for printing 1 is laminated on the thus formed printed circuit board 5. A method for laminating the mask for printing on the printed circuit board 5 is not particularly limited and, for example, mention may be made of a method of laminating the mask for printing 1 on the printed circuit board 5 (Fig. 7(c)) for adjusting respective alignment marks 4, 12 formed on both by arranging the mask for printing 1 and the printed circuit board 5 on a printing machine, recognizing the position of the alignment mark 4 formed on the mask for printing 1 with the use of a CCD camera 20 (Fig. 7(a)), then recognizing the alignment mark 12 formed on the printed circuit board 5 from the upper part of the printed circuit board 5 with the use of the CCD camera 20 (Fig. 7(b)), and correcting the position shift of the mask for printing 1 and the printed circuit board 5, and the like.

In case of this method, when the alignment mark 12 formed on the printed circuit board 5 is recognized, it is desirable to absorb or clamp-fix the printed circuit board 5 on a printing stage 21.

[0043]

Then, the cream solder 15 is filled in the opening portion 3 provided in the mask for printing 1 as shown in Fig. 1(c). The cream solder 15 can be any one commonly used without any particular limitation. As a typical example of the cream solder 15, for example, mention may be made of Sn63/Pb37, Sn62/Pb36/Ag2, Sn96.5/Ag3.5 and the like.

[0044]

After the cream solder 15 is filled in the

opening portion 3 provided in the mask for printing 1, as shown in Fig. 1(d), the mask for printing 1 is separated from the printed circuit board 5, thereby printing the cream solder 15 on the printed circuit board 5.

[0045]

After completing the printing, as shown in Fig. 1(e), a reflow treatment is applied to the printed cream solder 15, the solder bump 17 is formed, and thereafter the alignment mark 12 formed on the portion forming no conductor pattern in the vicinity of the outer peripheral portion of the printed circuit board is cut and removed by after-working, and the product portion A of the printed circuit board is cut in pieces.

[0046]

A method of solder printing the printed circuit board according to the invention is to form the alignment mark for positioning to the mask for printing on the portion in the vicinity of the outer peripheral portion of the printed circuit board where no conductor pattern is formed. Therefore, if the cream solder is printed on the alignment mark for positioning to the printed mask of the printed circuit board, the alignment mark for mounting IC chips is not solder printed, so that it is possible to recognize the alignment mark in case of mounting the IC chips.

[0047]

[Example]

The method of solder printing of the printed circuit board is further explained with reference to the example in detail as follows, but the invention is not limited to the example.

[0048]

(Example 1)

A cream solder is printed on the printed circuit board with the use of a mask for printing according to the printing method shown in Fig. 1.

[0049]

That is, in Fig. 1(a), as the mask for printing 1, use is made of a through-hole of 0.1 mm in diameter and 50 μ m in depth formed on the metal substrate 2 (340mm \times 255mm) having a thickness of 50 μ m comprised of nickel-cobalt alloy at the position corresponding to the alignment mark 12 of the printed circuit board, and the opening portion 3 having a circle of 100 μ m in diameter at the position corresponding to the pad 11 for forming a solder bump on the printed circuit board.

[0050]

Moreover, as the printed circuit board 5, use is made of a printed circuit board (340mm×255mm) taking 30 substrate (50mm×50mm) formed with a multilayered conductor circuit according to a build-up method.

The printed circuit board 5 concretely has the following construction. That is, the first layer conductor circuit 8 having a thickness of 20 μm as a source layer and the interlaminar insulating material 9 are formed on the insulating base 6 made from bismaleimide- triazine resin substrate having a thickness of 1 mm.

[0051]

The interlaminar insulating material 9 is an electroless plated adhesive having a thickness of 50 μm prepared by dispersing epoxy resin particles as a mixture of 35 parts by weight at 55 μm on average of particles and 5 parts by weight at 0.5 μm on average of particles in 70 parts by weight of epoxy acrylate resin, removing the epoxy resin particles with an oxidizing agent and applying a roughening treatment to the surface thereof. On the interlaminar insulating material 9 is formed a plating resist 10 of epoxy acrylate resin having a thickness of 20 μm , on the non-forming portion of the plating resist 10 is formed a viahole (pad 11 for forming a solder bump) connected to an inner layer as a part of a second layer conductor circuit having a diameter of 150 μm and an alignment mark 12 for positioning to a mask for printing 1 having a thickness of 20 μm and a diameter of 0.1 mm by electroless copper plating, and on the roughened layer 7 is applied electroless nickel-gold plating in the same manner. A needle-shaped alloy of copper-nickel-phosphorus is used for the roughened layer. As a forming method, it is immersed in an electroless plating aqueous solution comprising 8 g/l of copper sulfate, 0.6 g/l of nickel sulfate, 15 g/l of citric acid, 29 g/l of sodium hypophosphite, 31 g/l of boric acid and 0.1 g/l of surfactant and having pH=9 and deposited a thickness of about 3 μm on the surfaces of the alignment mark and the conductor circuit. Moreover, the nickel-gold layer is immersed in an electroless nickel plating solution of pH=5 comprising 30 g/l of nickel chloride, 10 g/l of sodium hypophosphite and 10 g/l of sodium citrate for 20 minutes to form a nickel plated layer having a thickness of 5 μm in the opening portion, further the substrate is immersed in an electroless plating solution

comprising 2 g/l of potassium gold cyanide, 75 g/l of ammonium chloride, 50 g/l of sodium citrate and 10 g/l of sodium hypophosphite at 93°C for 23 seconds to form a gold plated layer having a thickness of 0.03 μ m on the nickel plated layer. Moreover, a solder resist layer 14 having a thickness of 20 μ m is formed on the plating resist 10 for protecting the portion except the alignment mark 12 and the pad 11 for forming a solder bump. Further, the alignment mark 12 is provided at two places within 5 mm from both ends of one diagonal of the printed circuit board 5, and 100 pads 11 for forming a solder bump are formed on the printed circuit board 5 at intervals of 0.25 mm. Further, the alignment mark 13 for mounting IC chips is provided at two places within 7 mm from both ends of the diagonal with each substrate.

[0052]

Then, the mask for printing 1 and the printed circuit board 5 are provided on a printing machine, respective positions of the alignment mark 4 formed in the mask for printing 1 and the alignment mark 12 formed in the printed circuit board 5 are recognized with the use of a CCD camera 20, the positions of the mask for printing 1 and the printed circuit board 5 are adjusted, the mask for printing 1 is laminated on the printed circuit board 5 to adjust both the alignment marks, thereafter the cream solder 15 is filled in the opening portion 3 of the mask for printing 1 as shown in Fig. 1(b), and the mask for printing 1 is separated from the printed circuit board 5 as shown in Fig. 1(c) to print the cream solder 15 on the printed circuit board 5.

[0053]

After the completion of printing, the cream solder 15 is heated at 230°C. to make a solder bump 17. The printed circuit board is cut with each substrate and washed by removing powder to form a semiconductor package substrate (product) of 50 mm \times 50 mm.

[0054]

[Effect of the Invention]

According to a method of printing a solder on a printed circuit board, as an alignment mark for positioning to a mask for printing is formed on a portion in the vicinity of an outer peripheral portion of the printed circuit board where no conductor pattern is formed, even when a cream solder is printed on the alignment mark, each package substrate after cutting can use an alignment mark for mounting IC chips in case of mounting IC chips because the alignment mark for

mounting IC chips is not solder printed.

[Brief Description of the Drawings]

[Fig. 1]

An explanatory view showing one embodiment of a method for printing a solder on a printed circuit board according to the invention

[Fig. 2]

A plan view of a printed circuit board according to the invention

[Fig. 3]

A cross section of an alignment mark for positioning to a mask for printing.

[Fig. 4]

A cross section of an alignment mark for positioning to a mask for printing.

[Fig. 5]

A cross section of an alignment mark for positioning to a printed mask obtained by a semi-additive process.

[Fig. 6]

A plan view of a printed circuit board according to the prior art.

[Fig. 7]

A flow chart for positioning a printed mask and a printed circuit board.

[Explanation of the Signs]

- 1 mask for printing
- 2 metal substrate
- 3 opening portion
- 4 alignment (printed mask)
- 5 printed circuit board
- 6 insulating material
- 7 roughened layer
- 8 first layer conductor circuit
- 9 interlaminar insulating material
(adhesive layer for electroless plating)
- 10 plating resist
- 11 pad for solder bump formation
- 12 alignment mark
(used for positioning to a mask for printing)
- 13 alignment mark
(used for positioning in the mounting of an IC chip)

- 14 solder resist layer
- 15 cream solder
- A product portion
- 16 metal layer of nickel-gold
- 17 solder bump
- 18 electrolytic plated film
- 19 electroless plated film
- 20 CCD camera
- 21 printing stage
- 120 conductor layer for composing an alignment mark
- 130 alignment mark for mounting an IC chip

[Name of the Document] Abstract

[Subject]

To enable an IC chip to mount even when a cream solder is printed on an alignment mark for positioning to a printed circuit board.

[Solution]

A method of forming a solder bump on a printed circuit board comprising steps of laminating a printed mask provided with an alignment mark for positioning an opening for solder printing and a printed circuit board on the printing circuit board provided with an alignment mark for positioning the printed mask, aligning both the alignment marks, printing a cream solder on a semiconductor element mounting portion of the printed circuit board, heating and solder-melting to form a solder bump on the printed circuit, characterized in that the alignment mark provided on the printed mask is a through-hole, and, the alignment mark provided on the printed circuit board is formed on a portion forming no conductor pattern in the vicinity of an outer peripheral portion of the printed circuit board, and a printed circuit board and a printed mask used for the method.

[Selected Drawing] none